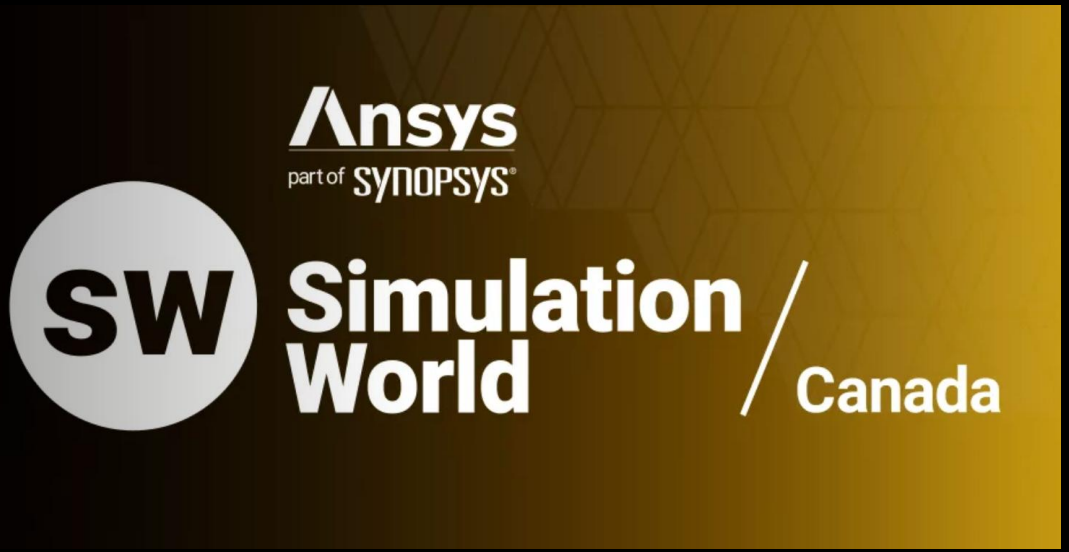

From Smooth to Imperfect Vias: The Rough Truth Impacting Simulation Model Accuracy

Bert Simonovich, Lamsim Enterprises Inc.

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May 26th, 2026

Lamsim Enterprises inc.

Innovative Signal Integrity & Backplane Solutions

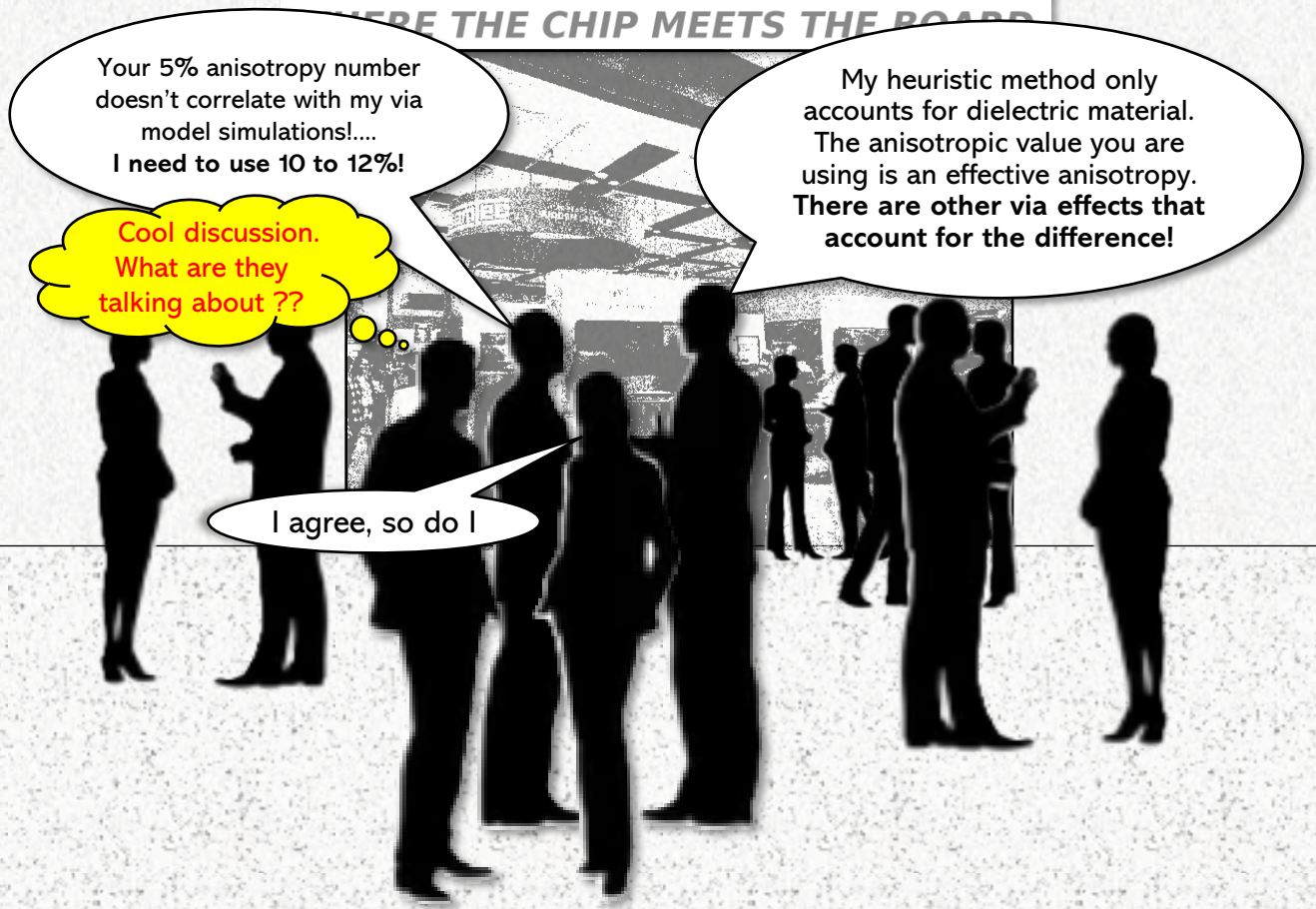
Abstract

The anisotropy of glass-reinforced laminates influences dielectric properties along different axes, depending on the direction of the electric field. Beyond material anisotropy, factors such as resin content, fabricated dielectric thicknesses, and drilled hole size contribute to variations in the effective dielectric constant surrounding via structures. Additionally, via barrel roughness affects both Dkeff and time delay, further complicating accurate dielectric modeling. This study examines the challenges of determining true material anisotropy from via stub resonant structures and introduces a heuristic approach to improve via simulation model accuracy.

Bio

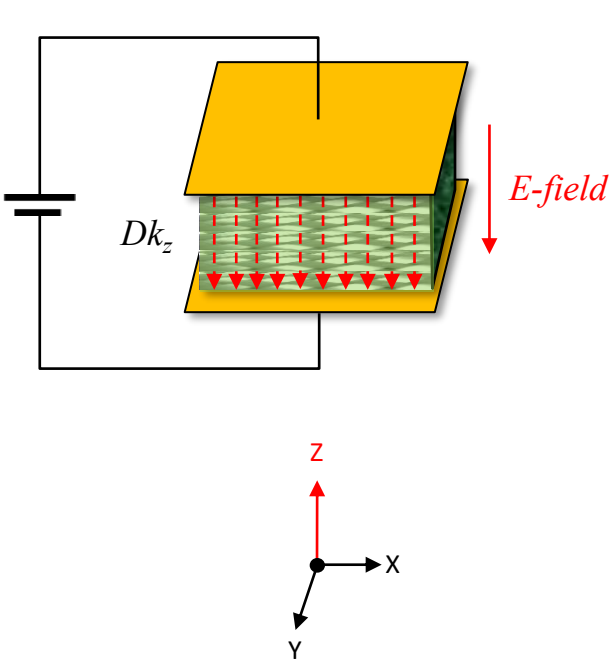
Lambert (Bert) Simonovich graduated from Mohawk College of Applied Arts and Technology as an Electronic Engineering Technologist. During his 32-year tenure at Bell Northern Research & Nortel in Ottawa Canada, he helped pioneer several advanced technologies into products. He has held a variety of engineering, research and development positions, eventually specializing in high-speed signal integrity and backplane design. In 2009, he founded Lamsim Enterprises Inc., and continues to provide innovative signal integrity and backplane solutions as a consultant. He has authored several publications, and in 2026 he was named DesignCon's Engineer of the Year. In addition to being a senior member of IEEE, he currently serves as a member of DesignCon's Technical Program Committee and Signal Integrity Journal's Editorial Advisory Board. His current research interests include high-speed signal integrity, modeling and characterization of high-speed serial link architectures, and holds two US patents. His most notable modeling achievement is the invention of the "Cannonball" conductor roughness model used in conjunction with the Huray model, used in several electronic design automation (EDA) software tools.

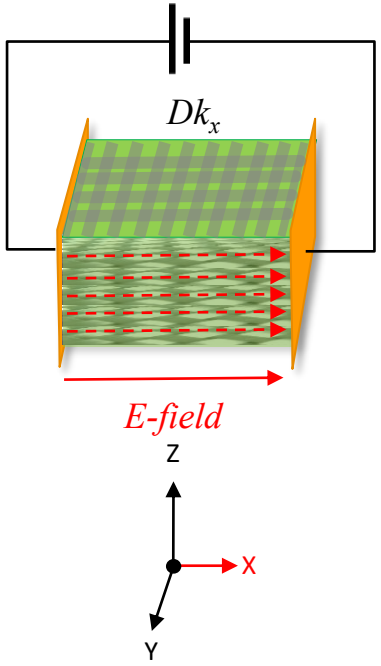
DESIGNCON® 2025

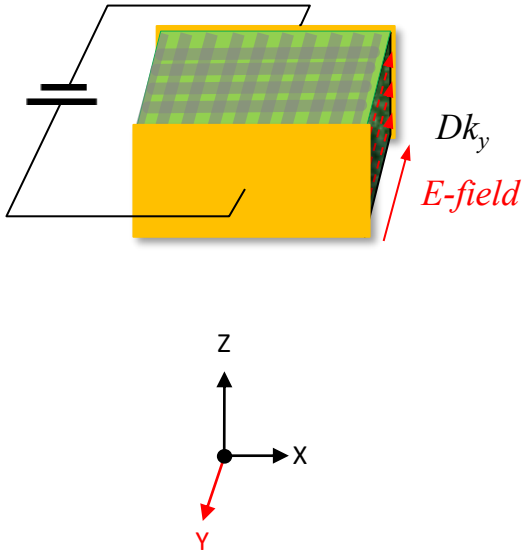


Anisotropy Overview

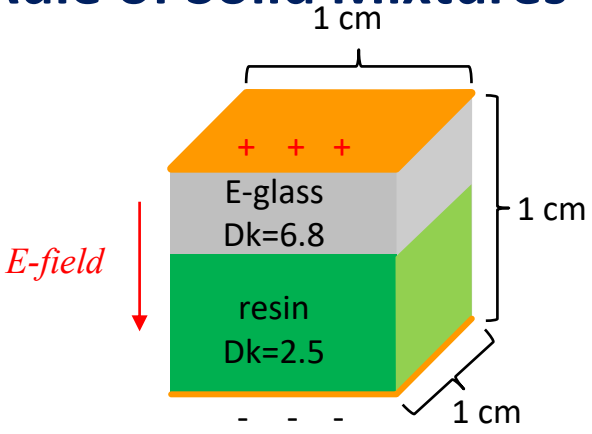
All Glass Reinforced Laminates are Anisotropic



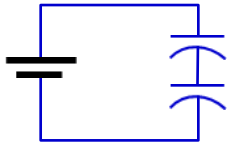




Rule of Solid Mixtures

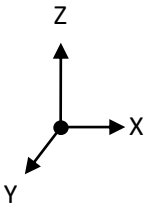


Cmix = CgCr/(Cg+Cr)



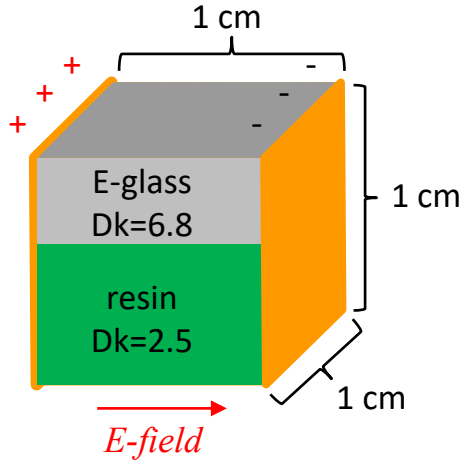
Parallel Mixing Rule

$$Dk_z = \left[v_{resin} / Dk_{resin} + v_{glass} / Dk_{glass} \right]^{-1}$$
$$= \left[0.7 / 2.5 + 0.3 / 6.8 \right]^{-1} = 3.09$$

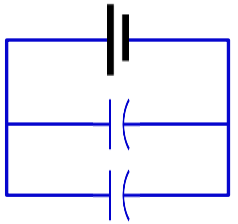


$$v_{resin} = 0.7cm^3$$
$$v_{glass} = 0.3cm^3$$
$$v_{mix} = 1.0cm^3$$

$$\Lambda = \left(\frac{Dk_{xy}}{Dk_z} - 1 \right) \cdot 100$$
$$= \left(\frac{3.79}{3.09} - 1 \right) \cdot 100 \approx 23\%$$



Cmix = Cg+ Cr

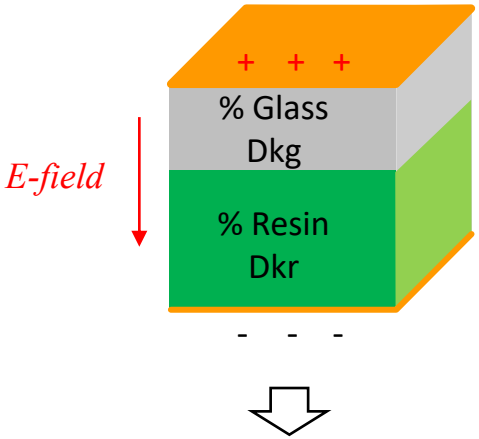


Series Mixing Rule

$$Dk_{xy} = v_{resin} \cdot Dk_{resin} + v_{glass} \cdot Dk_{glass}$$
$$= 0.7 \cdot 2.5 + 0.3 \cdot 6.8 = 3.79$$

P. S. Neelakanta, "Handbook of Electromagnetic Materials: Monolithic and Composite Versions and Their Applications", CRC Press LLC,1995

Heuristically Convert Dkz to Dkxy



$$Dk_z = \left[\left(1 - GC_v\right) / Dk_{resin} + GC_v / Dk_{glass} \right]^{-1}$$

Parallel Mixing Rule

1. Determine Dkresin:

$$Dkr = \frac{Dkz\left(1 - GC_v\right)}{\left(1 - \left(\frac{DkzGC_v}{Dkg}\right)\right)}$$

2. Determine Dkxy:

$$Dkxy = \left(1 - GC_v\right) Dkr + \left(GC_v\right) Dkg$$

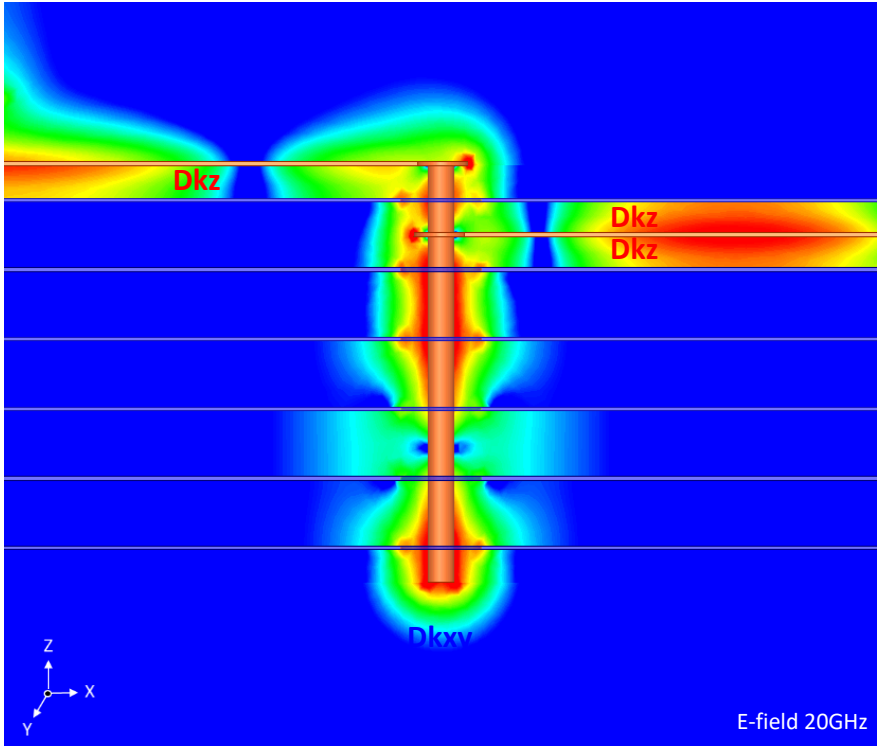
Tachyon 100G Construction Table Dk Anisotropy*

Glass Style	Resin Content %	Offering	Thickness (inch)	Thickness (mm)	Dielectric Constant (Dkz)						Dkxy						Anisotropy
					1 GHz	2 Ghz	5 Ghz	10 GHz	15 Ghz	20 Ghz	1 GHz	2 Ghz	5 Ghz	10 GHz	15 Ghz	20 Ghz	xy:z
1035	69.00%	Standard	0.002	0.051	3.06	3.06	3.06	3.06	3.06	3.06	3.23	3.23	3.23	3.23	3.23	3.23	5.6%
1035	75.00%	Standard	0.0026	0.066	2.97	2.97	2.97	2.97	2.97	2.97	3.11	3.11	3.11	3.11	3.11	3.11	4.7%
1078	65.00%	Standard	0.0029	0.074	3.14	3.14	3.14	3.14	3.14	3.14	3.31	3.31	3.31	3.31	3.31	3.31	5.5%
1078	67.50%	Standard	0.0031	0.079	3.09	3.09	3.09	3.09	3.09	3.09	3.26	3.26	3.26	3.26	3.26	3.26	5.5%
1078	70.50%	Standard	0.0035	0.089	3.04	3.04	3.04	3.04	3.04	3.04	3.20	3.20	3.20	3.20	3.20	3.20	5.1%
1078	72.00%	Standard	0.0037	0.094	3.02	3.02	3.02	3.02	3.02	3.01	3.17	3.17	3.17	3.17	3.17	3.16	5.0%
1078	75.00%	Standard	0.0042	0.107	2.97	2.97	2.97	2.97	2.97	2.97	3.11	3.11	3.11	3.11	3.11	3.11	4.6%
1078	78.00%	Alternate	0.0046	0.117	2.92	2.92	2.92	2.92	2.92	2.92	3.05	3.05	3.05	3.05	3.05	3.05	4.5%
2116	62.00%	Standard	0.0058	0.147	3.19	3.19	3.19	3.19	3.19	3.19	3.37	3.37	3.37	3.37	3.37	3.37	5.7%
2116	65.00%	Alternate	0.0064	0.163	3.14	3.14	3.14	3.14	3.14	3.14	3.31	3.31	3.31	3.31	3.31	3.31	5.4%
1067	70.00%	Standard	0.0022	0.056	3.05	3.05	3.05	3.05	3.05	3.05	3.21	3.21	3.21	3.21	3.21	3.21	5.2%
1067	71.50%	Standard	0.0024	0.061	3.02	3.02	3.02	3.02	3.02	3.02	3.17	3.17	3.17	3.17	3.17	3.17	4.9%
1067	74.00%	Standard	0.0026	0.066	2.98	2.98	2.98	2.98	2.98	2.98	3.12	3.12	3.12	3.12	3.12	3.12	4.8%
1067	76.50%	Standard	0.0029	0.074	2.94	2.94	2.94	2.94	2.94	2.94	3.07	3.07	3.07	3.07	3.07	3.07	4.4%
106	76.00%	Standard	0.0023	0.058	2.95	2.95	2.95	2.95	2.95	2.95	3.08	3.08	3.08	3.08	3.08	3.08	4.4%
1080	72.00%	Standard	0.0038	0.097	3.02	3.02	3.02	3.02	3.02	3.01	3.16	3.16	3.16	3.16	3.16	3.15	4.7%
1080	75.00%	Standard	0.0043	0.109	2.97	2.97	2.97	2.97	2.97	2.97	3.10	3.10	3.10	3.10	3.10	3.10	4.4%
1080	78.00%	Alternate	0.0046	0.117	2.92	2.92	2.92	2.92	2.92	2.92	3.05	3.05	3.05	3.05	3.05	3.05	4.4%
3313	63.50%	Standard	0.0046	0.117	3.16	3.16	3.16	3.16	3.16	3.16	3.35	3.35	3.35	3.35	3.35	3.35	5.9%
3313	66.50%	Standard	0.0051	0.129	3.11	3.11	3.11	3.11	3.11	3.11	3.28	3.28	3.28	3.28	3.28	3.28	5.6%

Bulk Dk anisotropy varies 4.4% – 5.9 % depending on glass style and resin content

* Ref: Bert Simonovich, “A Heuristic Approach to Assess Anisotropic Properties of Glass-reinforced PCB Substrates”, DesignCon 2024 proceedings, Santa Clara, CA

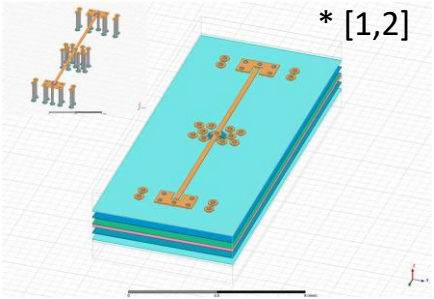
Dk Anisotropy Implications for Via Modeling



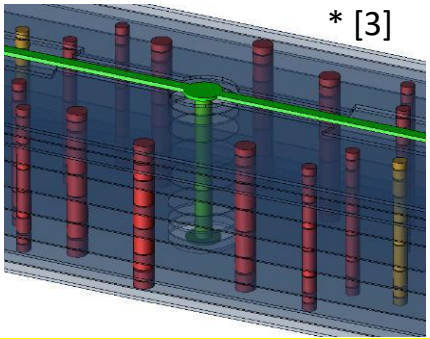
	Dkxy	Dkz
Trace Impedance	✗	✓
Via Impedance	✓	✗
Via Stub Resonance	✓	✗

HFSS simulation courtesy of Juliano Mologni, Ansys

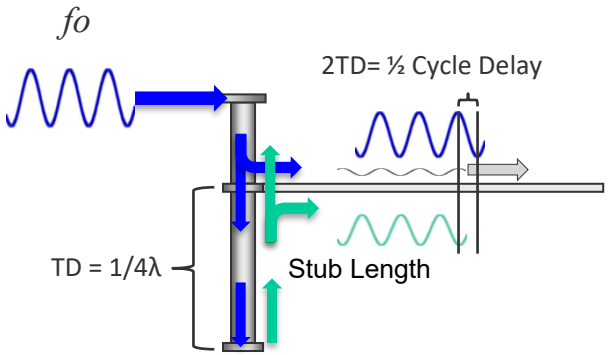
Experimental Attempts to Extract Dielectric Anisotropy based on 1/4 – wave Resonant Via Structures

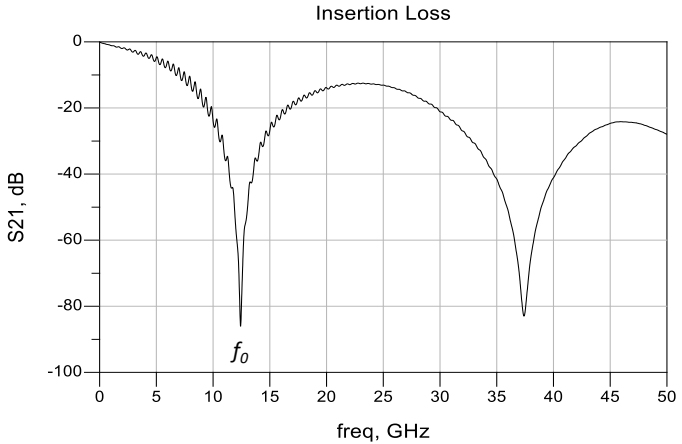


* [1,2]



* [3]





$$f_0 = \frac{c}{4 \times stublength \times \sqrt{Dkeff}}$$

$$Dkeff = \left(\frac{c}{4 \times stublength \times f_0} \right)^2$$

Since resonant freq. is highly dependent on phase delay (TD) any change in via geometry will affect Dkeff

[1] Scott McMorrow et al, "Anisotropic Design Considerations for 28 Gbps Via to Stripline Transitions", DesignCon 2015 proceedings, Santa Clara, CA;
[2] Scott McMorrow, "Anisotropy Test Vehicle Tachyon Results", Samtec presentation, 2022;
[3] Al Neves et al, "Free Signal Integrity? How Understanding Anisotropic Materials & Tolerances Could Increase Performance at 112/224Gbps & Beyond", DesignCon 2025 proceedings, Santa Clara, CA

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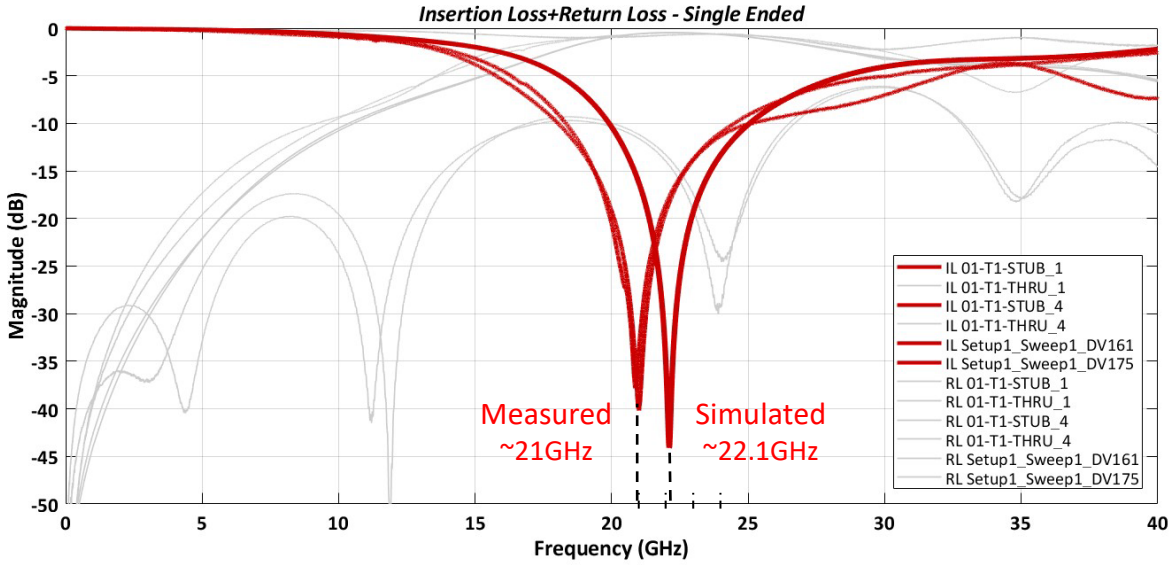
Experimental Results [1,2]



$$Dkeff_{meas} = \left(\frac{1.18E10}{4\times 21.0E9\times 74.4E-3}\right)^2 \cong 3.6$$

$$Dkeff_{sim} = \left(\frac{1.18E10}{4\times 22.1E9\times 74.4E-3}\right)^2 \cong 3.2$$

$$\Lambda_{eff} = \frac{3.6}{3.2} - 1 = 12.5\%$$

This is effective Anisotropy!

PCB stackup manufacturing process variations not considered

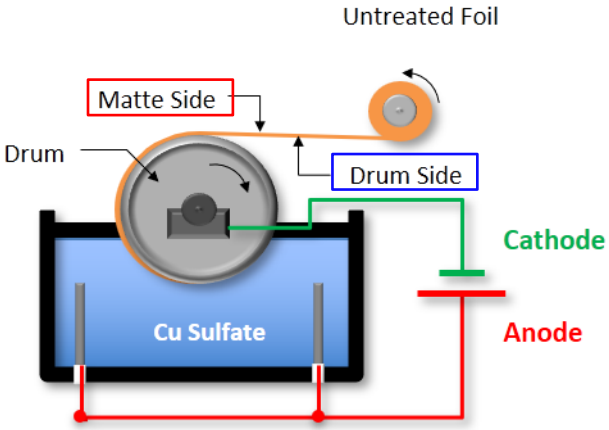
PCB drill size used compared to simulation model not considered

Via roughness not considered

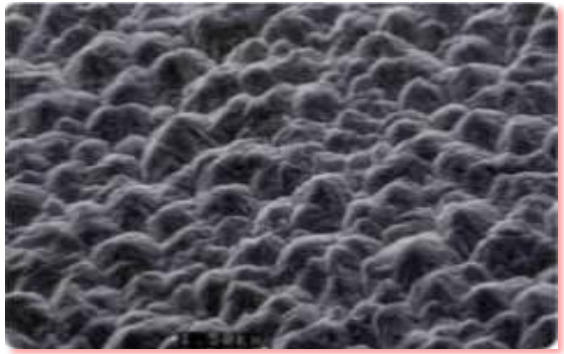
Ref: [1] Scott McMorrow et al, "Anisotropic Design Considerations for 28 Gbps Via to Stripline Transitions", DesignCon 2015 proceedings, Santa Clara, CA.
[2] Scott McMorrow, "Anisotropy Test Vehicle Tachyon Results", Samtec presentation, 2022

Conductor Roughness

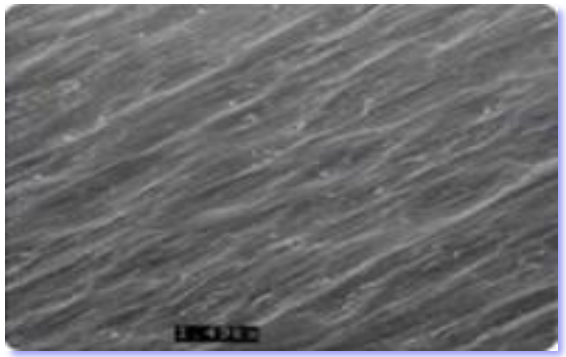
Electrodeposited Conductor Roughness



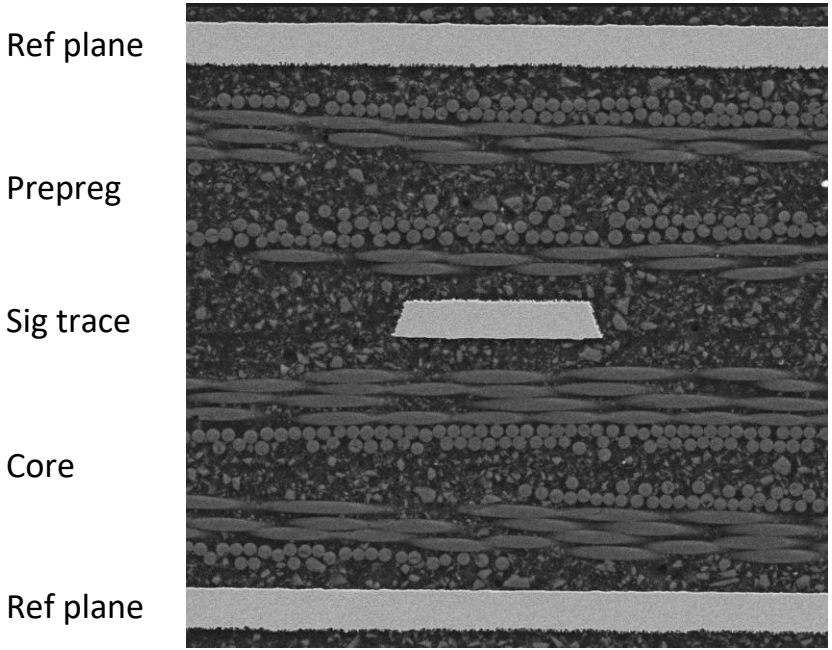
Matte Side



Drum Side

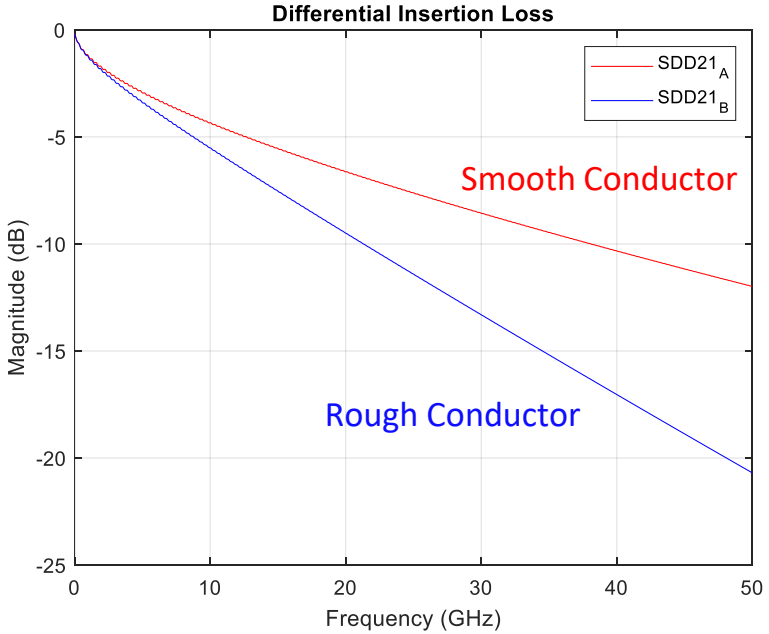


PCB Transmission Lines



- All traces and reference planes will have surface roughness to promote adhesion to dielectric material
- Conductor roughness increases transmission loss and phase or time delay (TD)

Modeling Conductor Surface Roughness Loss Effect



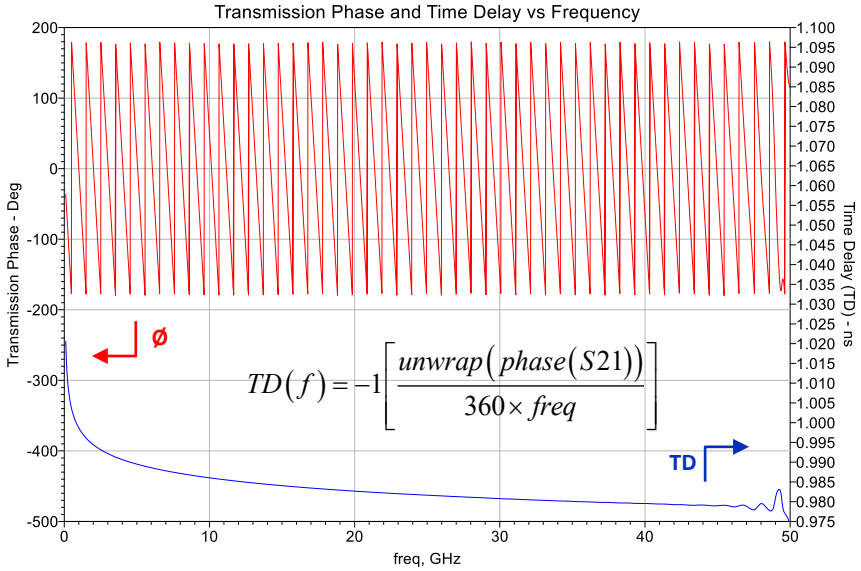
$$IL_{total}(f) = IL_{conductor}(f) + IL_{diel}(f)$$

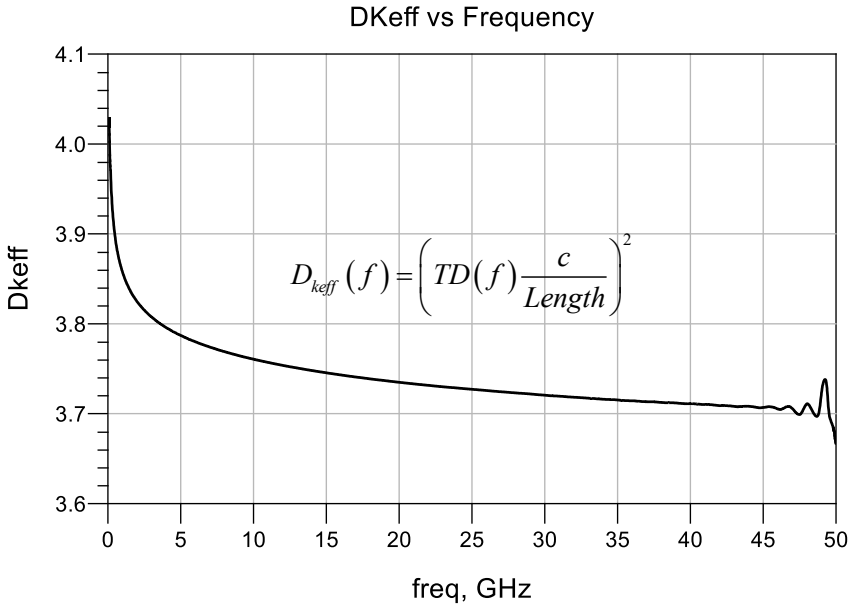
$$IL_{total}(f) = K_{SR}(f) \times IL_{conductor}(f) + IL_{diel}(f)$$

Surface Roughness Correction Coefficient

- Cannonball Model
- Huray Model
- Hammerstad-Jensen Model
- Groiss Model

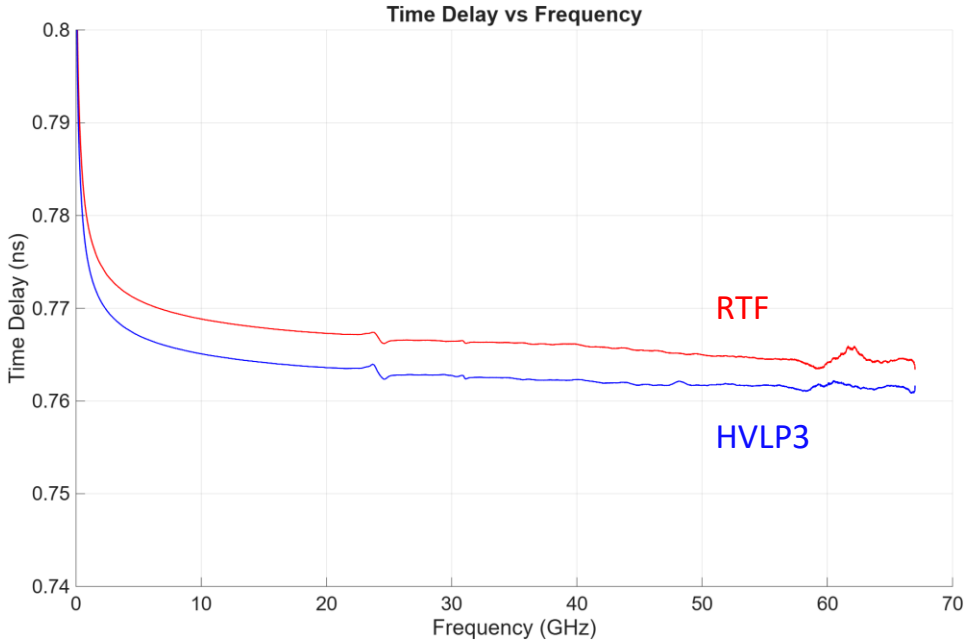
Effective Dk from Phase Delay (TD)





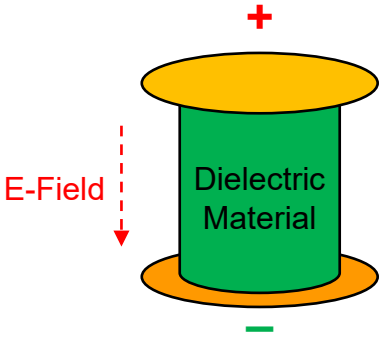
TD often used to determine Dkeff

Transmission Time Delay due to Conductor Foil Roughness

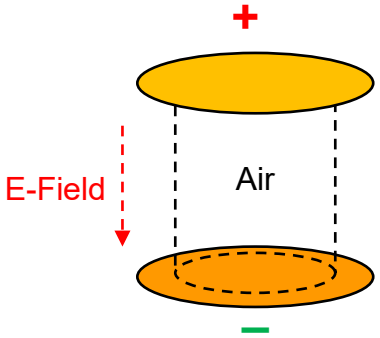


Roughness of foil increases transmission line phase delay (TD)

Effective Dielectric Constant Dkeff

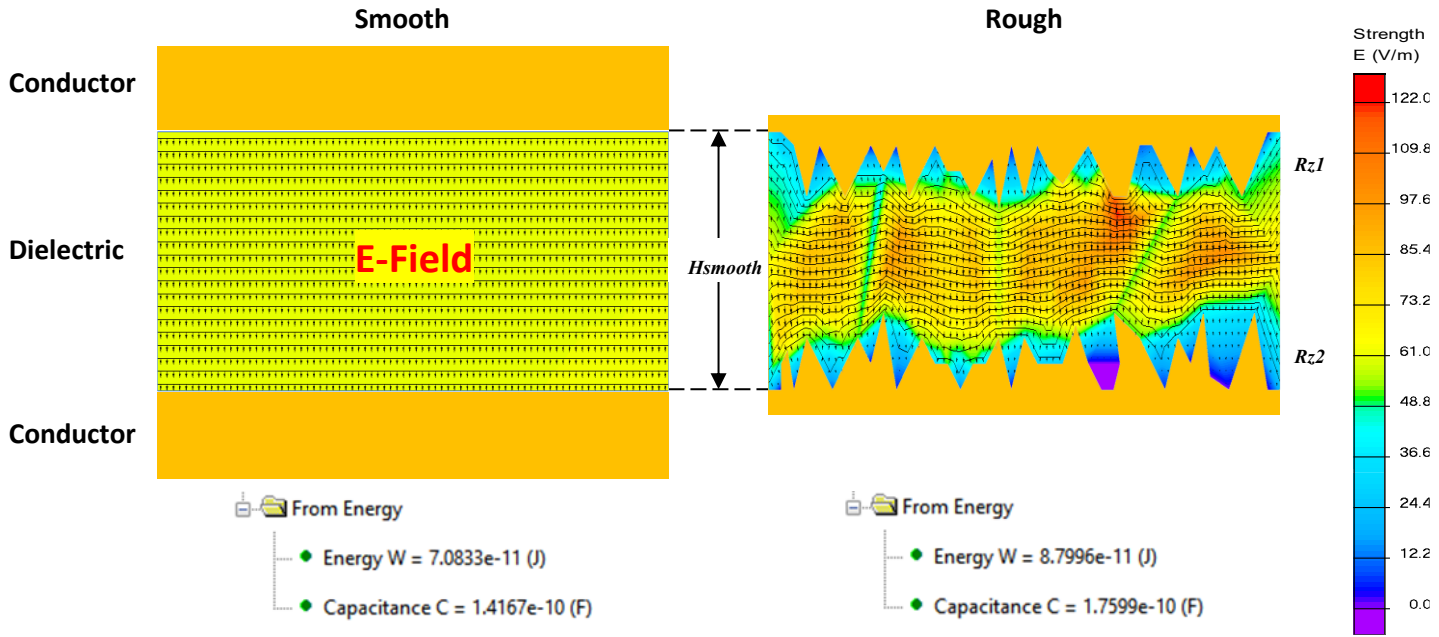


$$Dkeff = \frac{C_{actual}}{C_{air}}$$



Dk is the ratio of actual structure's capacitance to the capacitance of an identical structure when dielectric material is replaced by air or vacuum.

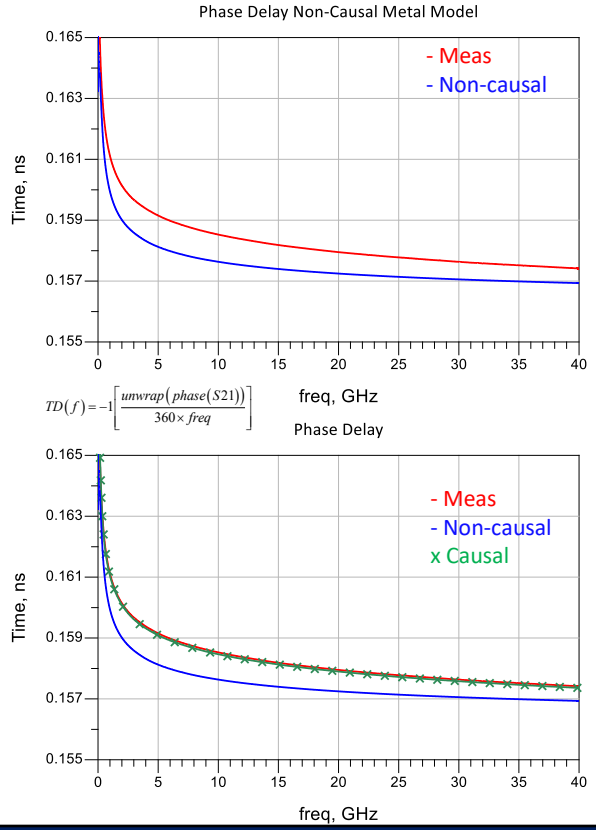
Capacitance due to PCB Conductor Roughness



$$Dk_{eff} = \frac{H_{smooth}}{\left(H_{smooth} - \left(R_{z1} + R_{z2}\right)\right)} \times Dk$$

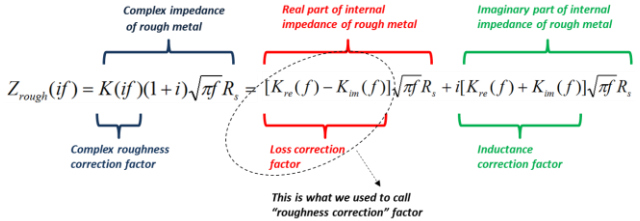
Conductor roughness increases capacitance resulting in a higher effective Dk (Dkeff)

Trace Self Inductance due to PCB Conductor Roughness



Conductor roughness increases trace self inductance thereby increasing phase delay

- Using a non-causal metal model does not account for additional phase delay caused by conductor roughness

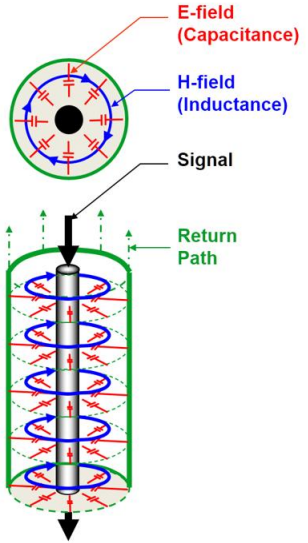


Roughness correction factor must be added to the real part of the internal impedance of rough metal as well as an inductance correction factor to the imaginary part to ensure causality*

- Need to use Bracken model or equivalent

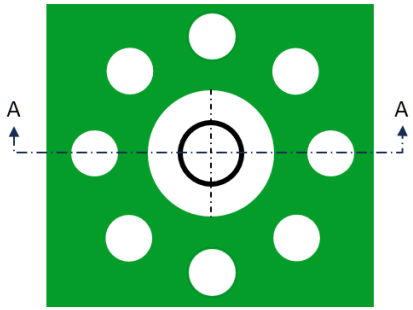
* Ref: V. Dmitriev-Zdorov, B. Simonovich, Igor Kochikov, "A Causal Conductor Roughness Model and its Effect on Transmission Line Characteristics", DesignCon 2018 Proceedings, Santa Clara, CA, 2018

Localized Via Structure

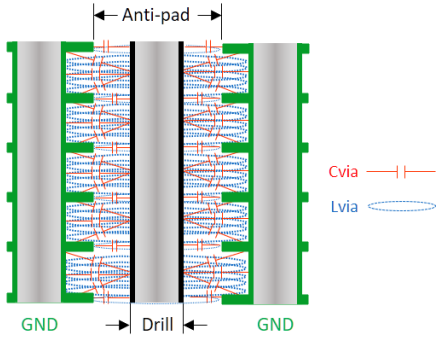


$$Ccoax = \frac{2\pi\varepsilon_0}{\ln\left(\frac{Shield\phi}{Conductor\phi}\right)} \times \varepsilon_r$$

$\cong$



Top View

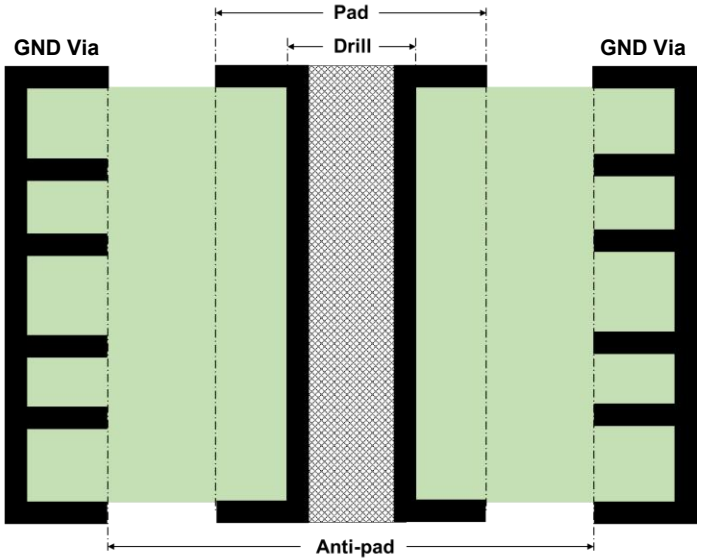


Section A-A

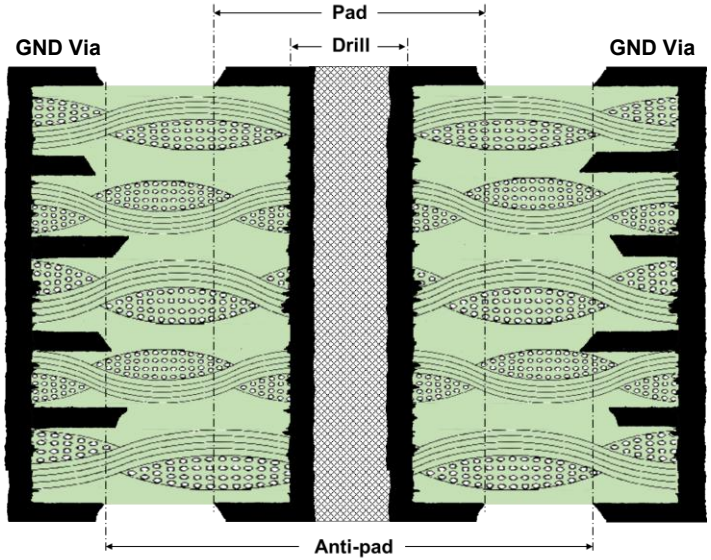
$$Cvia \cong \frac{2\pi\varepsilon_0}{\ln\left(\frac{Antipad\phi}{Drill\phi}\right)} \times Dkxy$$

- Resembles coaxial structure
- Circular GND vias localize EM-field
- Via capacitance mainly influenced by Drillϕ, Antipadϕ & GND vias in close proximity

Via Model vs Reality

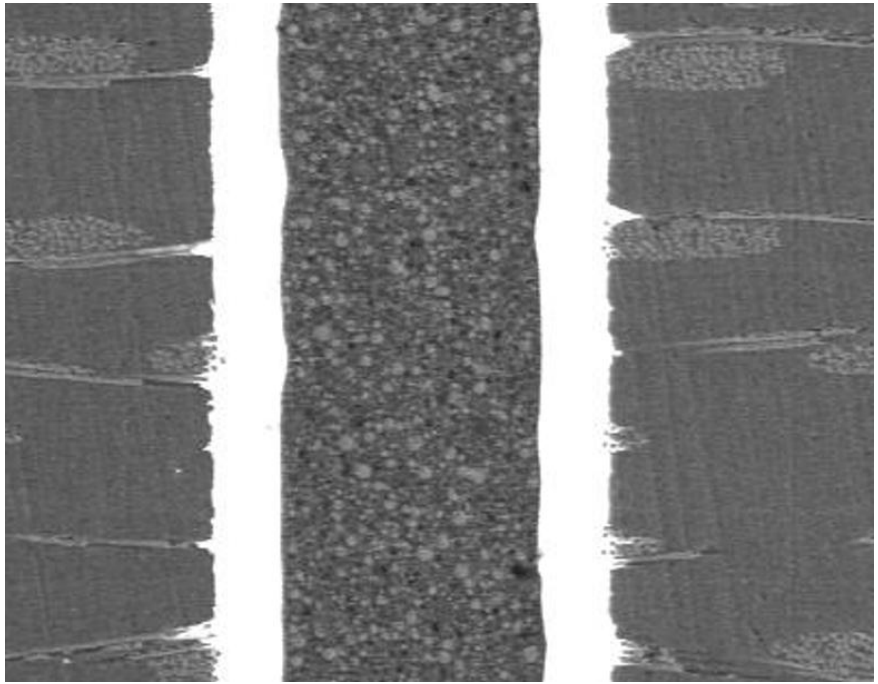


- Smooth via barrel
- Anti-pads perfectly aligned all layers
- Drill size is same as imported from CAD (FHS)
- Dk is same as imported from CAD file or as designed stackup



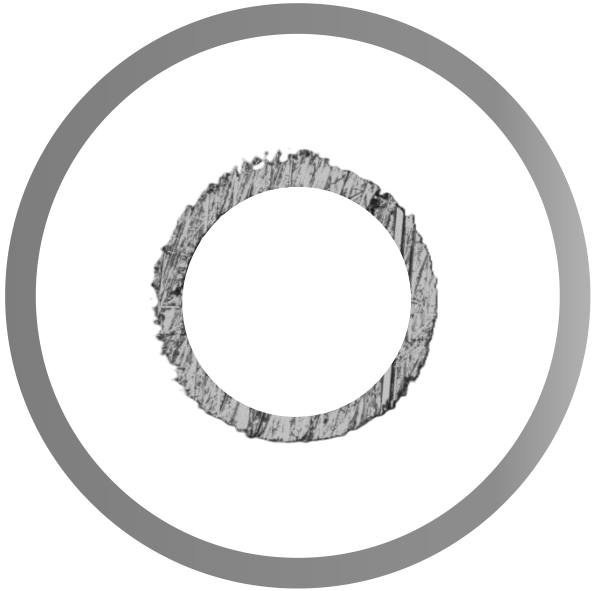
- Rough via barrel
- Anti-pads are not perfectly aligned all layers
- Drill size is actual drill & not FHS imported from CAD
- Dk is anisotropic & not same as imported from CAD file or as designed stackup

Main Cause of Via Barrel Roughness



Drilling through glass-reinforced laminates causes crazing allowing copper plating to wick into the voids

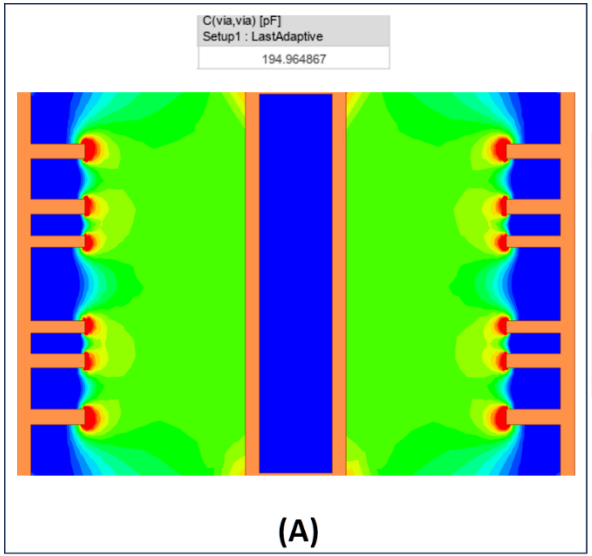
Via barrel is equivalent to a flat sheet of foil rolled into a cylinder

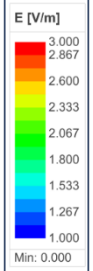


When combined with a reference planes roughness has same influence as PCB transmission line traces

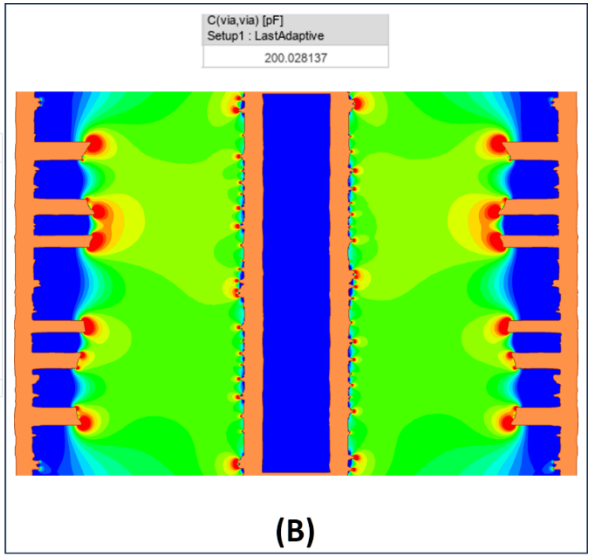
Via Barrel Roughness

Smooth Via



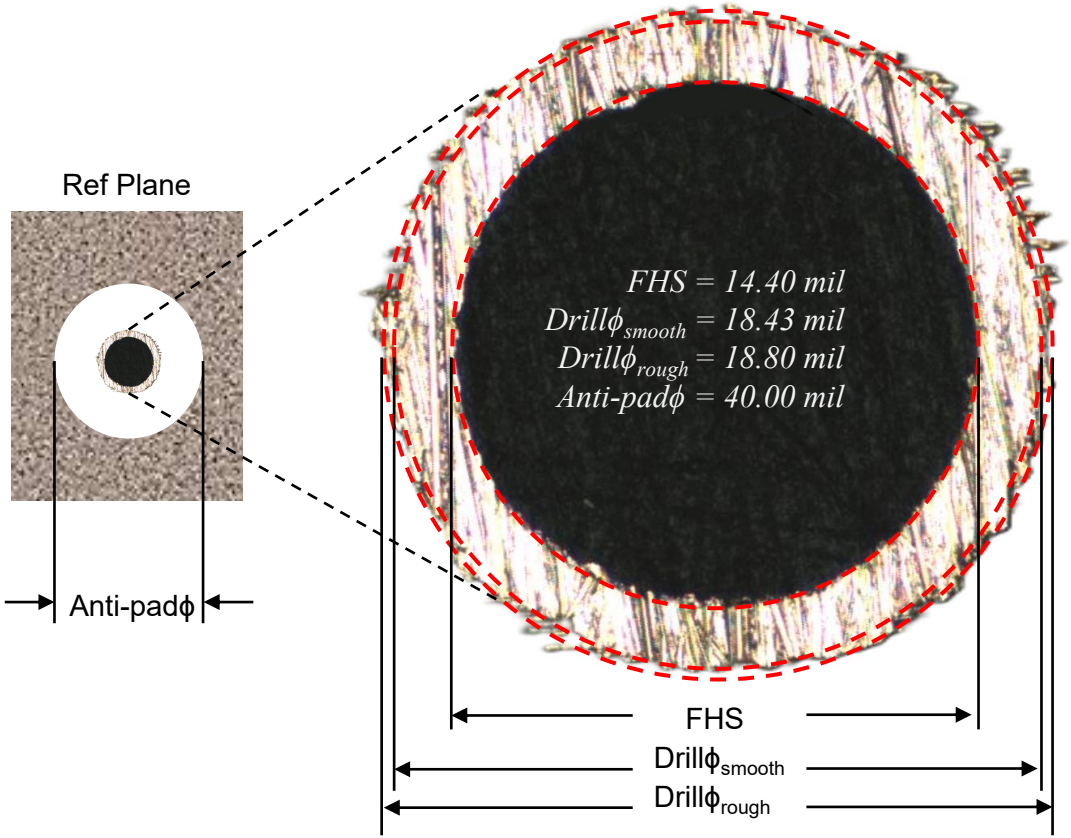


Rough Via



Via barrel roughness increases via capacitance resulting in higher Dkeff

Dkeff Compensation Due to Via Barrel Roughness Example



$$\frac{Dkeff_{rough}}{Dkeff_{smooth}} = \frac{Cvia_{rough}}{Cvia_{smooth}}$$

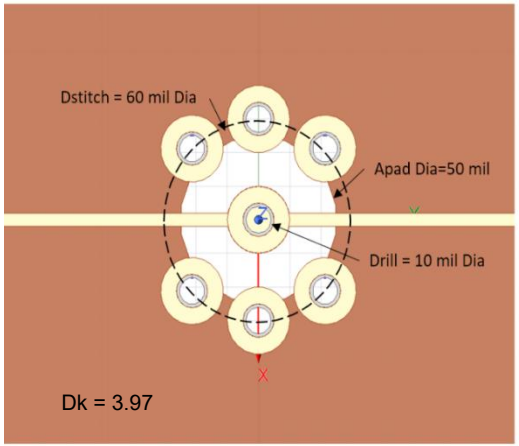
$$Dkeff_{rough} = \frac{Cvia_{rough}}{Cvia_{smooth}} \times Dkeff_{smooth}$$

$$\cong \frac{\ln\left(\frac{Antipad\phi}{Drill\phi_{smooth}}\right)}{\ln\left(\frac{Antipad\phi}{Drill\phi_{rough}}\right)} \times Dkeff_{smooth}$$

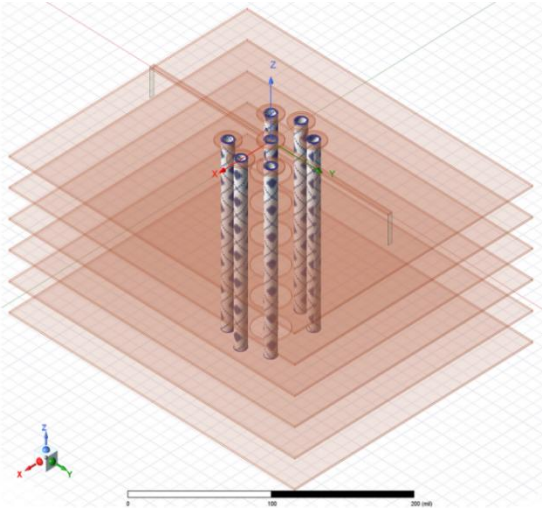
$$\cong \frac{\ln\left(\frac{40}{18.43}\right)}{\ln\left(\frac{40}{18.80}\right)} \times Dkeff_{smooth}$$

$$\cong 1.026 \times Dkeff_{smooth}$$

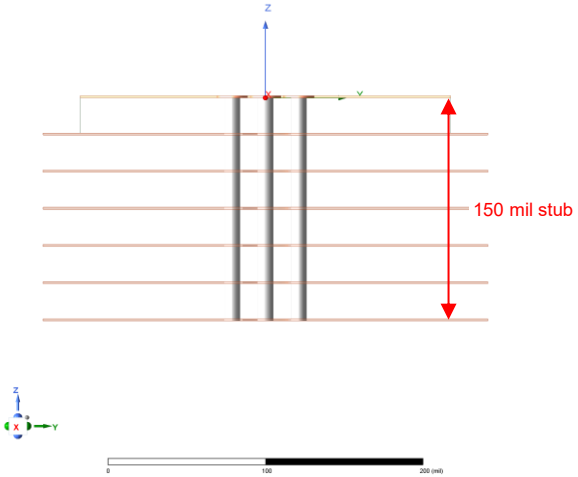
Via Delay due to Roughness HFSS Model Experiment



Top Down View

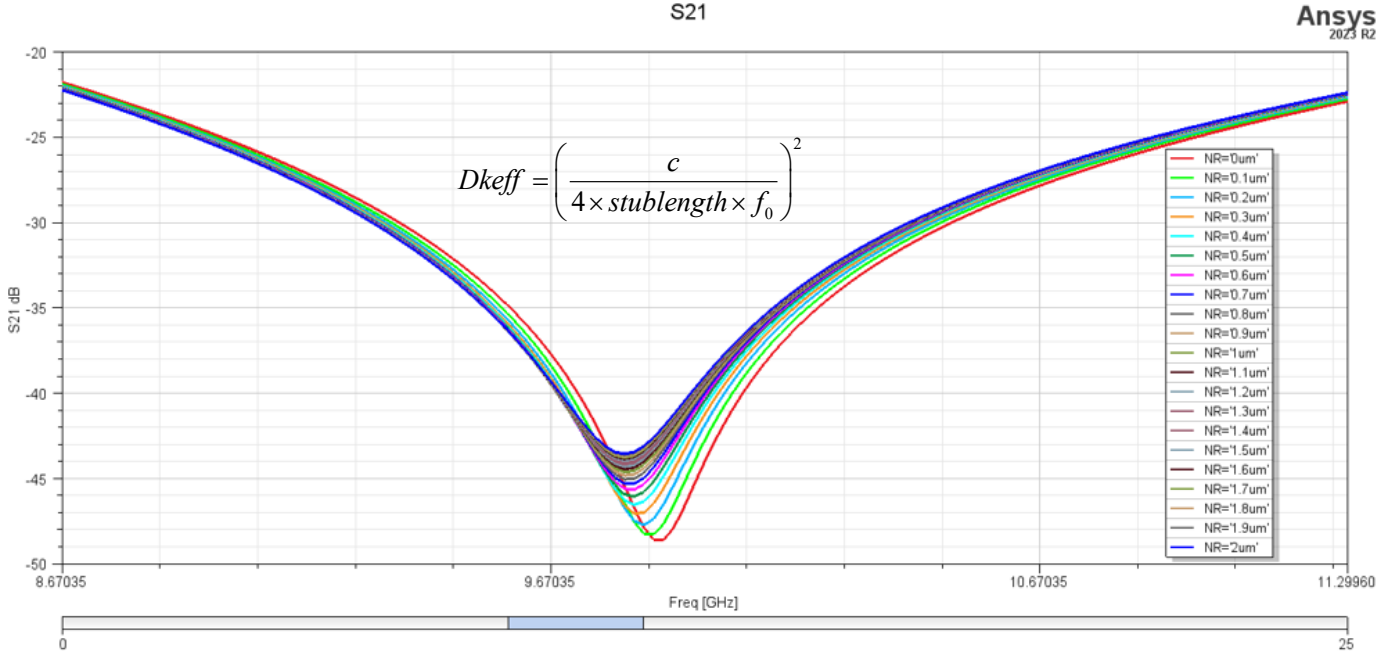


3D View



- Huray roughness model added to vias (causal Bracken model included)
- Huray NR parameterized from 0 to 2 µm in 0.1 µm (Rz = 0 to 33 µm) increments
- Via geometry fixed

Via Time Delay due to Roughness



f_0	TD ps	NR um	Rz um	Dkeff	Dkeff % Delta
9.900E+09	25.253	0.0	0.000	3.96744	0.00%
9.880E+09	25.304	0.1	1.667	3.98352	0.41%
9.860E+09	25.355	0.2	3.333	3.99970	0.81%
9.860E+09	25.355	0.3	5.000	3.99970	0.81%
9.840E+09	25.407	0.4	6.667	4.01597	1.22%
9.840E+09	25.407	0.5	8.333	4.01597	1.22%
9.840E+09	25.407	0.6	10.000	4.01597	1.22%
9.820E+09	25.458	0.7	11.667	4.03235	1.64%
9.820E+09	25.458	0.8	13.333	4.03235	1.64%
9.820E+09	25.458	0.9	15.000	4.03235	1.64%
9.820E+09	25.458	1.0	16.667	4.03235	1.64%
9.820E+09	25.458	1.1	18.333	4.03235	1.64%
9.820E+09	25.458	1.2	20.000	4.03235	1.64%
9.820E+09	25.458	1.3	21.667	4.03235	1.64%
9.820E+09	25.458	1.4	23.333	4.03235	1.64%
9.820E+09	25.458	1.5	25.000	4.03235	1.64%
9.820E+09	25.458	1.6	26.667	4.03235	1.64%
9.820E+09	25.458	1.7	28.333	4.03235	1.64%
9.820E+09	25.458	1.8	30.000	4.03235	1.64%
9.820E+09	25.458	1.9	31.667	4.03235	1.64%
9.820E+09	25.458	2.0	33.333	4.03235	1.64%

$$TD = \frac{\sqrt{Dkeff}}{c} \times stublength$$

$$\sqrt{L_{11}C_{11}} = \frac{\sqrt{Dkeff}}{c}$$

- Time-variant electromagnetic fields inductance also contributes to time delay (TD)
- Via barrel roughness affects the self-inductance (L11) in same way copper surface roughness increases L11 in transmission line geometries

HFSS simulation model courtesy of Juliano Mologni

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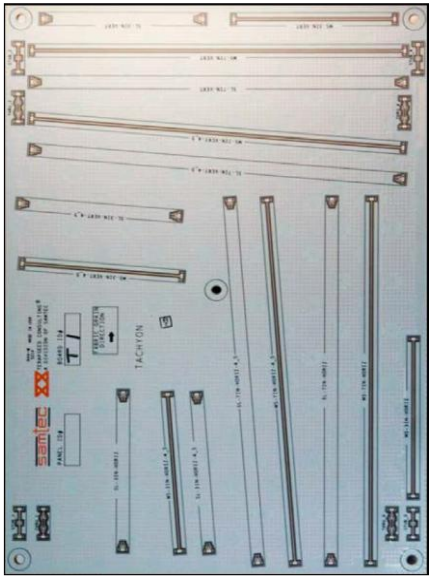
Previous Study

Test Vehicle



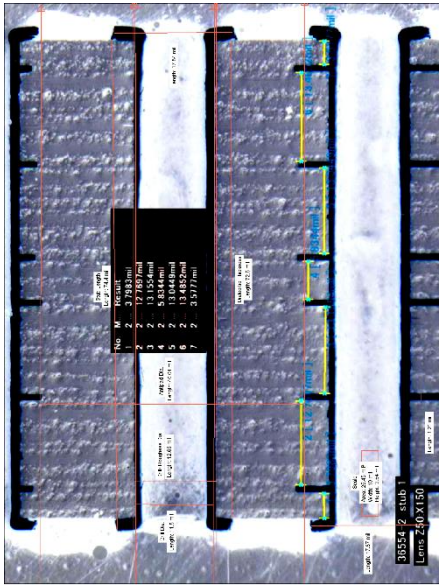
As Designed

Lyr	Thickness	Cross Section Diagram	Dk	Layer Definition	Material Type	Cu. & Diel. Tol.
	0.7			Resist		
	1.4			Cu Plating		
L01	0.6			Signal		0.5 oz.
	4.0	1 X 1078 - 75.5%	2.96	B-Stage		(+\- 1.0)
L02	0.6			Plane		0.5 oz.
	6.0	(2-1078) 0.006 H/O	3.05	Core		(+\- 1.0)
L03 - BLANK	0.0			Blank		0 oz.
	8.2	2 X 1078 - 75.5%	2.96	B-Stage		(+\- 1.0)
L04	0.6			Plane		0.5 oz.
	6.0	(2-1078) 0.006 H/O	3.05	Core		(+\- 1.0)
L05 - BLANK	0.0			Blank		0 oz.
	8.2	2 X 1078 - 75.5%	2.96	B-Stage		(+\- 1.0)
L06	0.6			Plane		0.5 oz.
	6.0	(2-1078) 0.006 H/H	3.05	Core		(+\- 1.0)
L07	0.6			Plane		0.5 oz.
	8.2	2 X 1078 - 75.5%	2.96	B-Stage		(+\- 1.0)
L08 - BLANK	0.0			Blank		0 oz.
	6.0	(2-1078) 0.006 O/H	3.05	Core		(+\- 1.0)
L09	0.6			Plane		0.5 oz.
	7.6	2 X 1078 - 75.5%	2.96	B-Stage		(+\- 1.0)
L10	0.6			Signal		0.5 oz.
	6.0	(2-1078) 0.006 H/H	3.05	Core		(+\- 1.0)
L11	0.6			Plane		0.5 oz.
	4.0	1 X 1078 - 75.5%	2.96	B-Stage		(+\- 1.0)
L12	0.6			Signal		0.5 oz.
	1.4			Cu Plating		
	0.7			Resist		
Total:	79.8	Est. Finish Thickness Over Mask		Tol: +/- 10%		(+/- 8.0)

TACHYON

≠

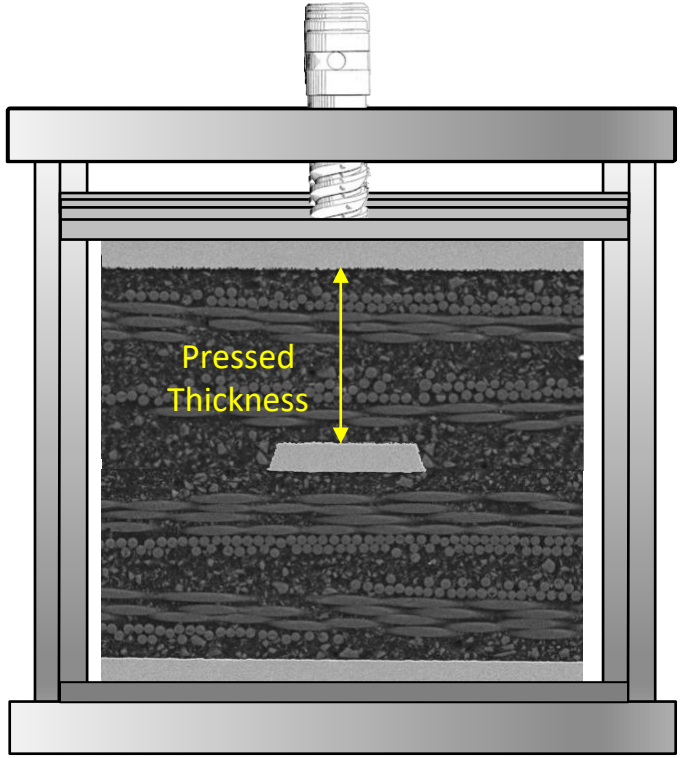
As Fabricated

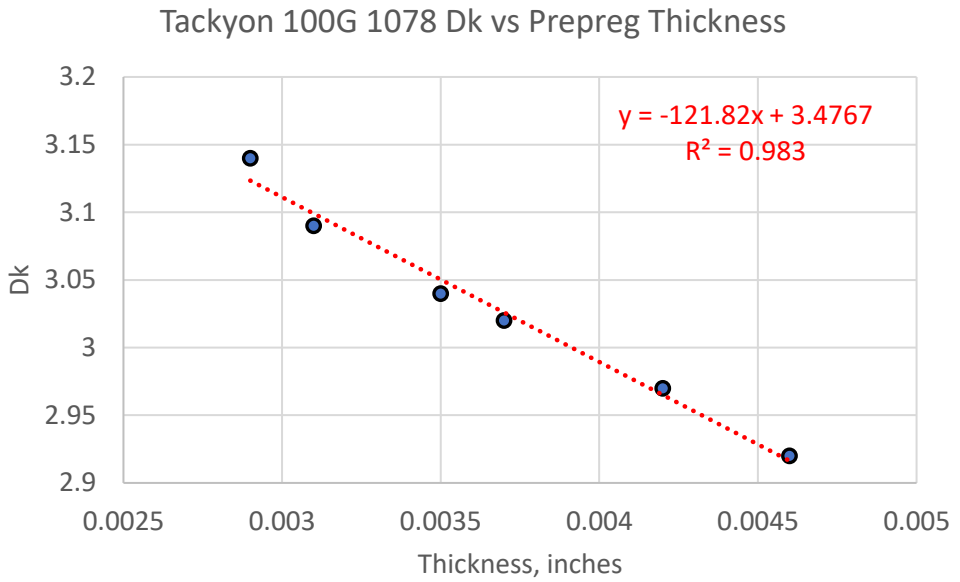


As fabricated stackup and via geometry not always the same as designed!

Ref: [1] Scott McMorrow et al, "Anisotropic Design Considerations for 28 Gbps Via to Stripline Transitions", DesignCon 2015 proceedings, Santa Clara, CA.
[2] Scott McMorrow, "Anisotropy Test Vehicle Tachyon Results", Samtec presentation, 2022

Pressed Dielectric Thickness Affect on Dk





Prepreg loses resin content as it is pressed resulting in higher Dk for pressed thickness

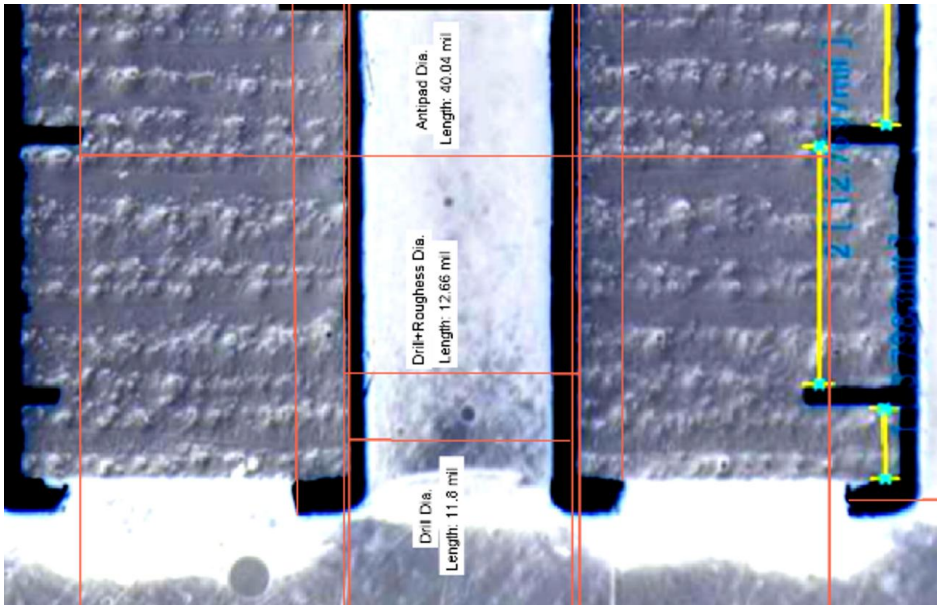
As-fabricated Dielectric Thickness Effect on Dielectric Constant

TABLE 1

No.	M		Stackup mil	Stackup mil	As Designed Dkz Stackup	As Designed Dkxy Calculated	X-sec Meas Thick mil	X-sec Stackup mil	Pressed Single ply thickness mils	Pressed Dkz X-sec (linear fit)	Pressed Dkxy Calculated	Pressed Anisotropy
1	2	Bstage		4	2.96	3.08	3.80	3.80	3.80	3.01	3.14	4.2%
2	2	core	14.2	6	3.05	3.21	12.77	5.8344	2.92	3.12	3.28	5.1%
		Bstage		8.2	2.96	3.10		6.9353	3.47	3.05	3.2	4.8%
3	2	core	14.2	6	3.05	3.21	13.16	5.8344	2.92	3.12	3.28	5.1%
		Bstage		8.2	2.96	3.10		7.321	3.66	3.03	3.17	4.6%
4	2	Core		6	3.05	3.21	5.83	5.8344	2.92	3.12	3.28	5.1%
5	2	Bstage	14.2	8.2	2.96	3.10	13.04	7.2105	3.61	3.04	3.18	4.7%
		Core		6	3.05	3.21		5.8344	2.92	3.12	3.28	5.1%
6	2	Bstage	13.6	7.6	2.96	3.08	13.49	7.6508	3.83	3.01	3.14	4.3%
		Core		6	3.05	3.21		5.8344	2.92	3.12	3.28	5.1%
7	2	Bstage		4	2.96	3.1	3.58	3.58	3.58	3.04	3.18	4.6%
Averages					3.00	3.14				3.07	3.22	4.9%

Pressed dielectric resin loss increases Dkxy

Dkeff Increase from Capacitance Due to Via Roughness



Drillϕ_{smooth} = 11.80 mil
Drillϕ_{rough} = 12.66 mil
Roughness ~ 0.43 mil (10.9 um)
Antipadϕ = 40.04 mil
Dkeffxy$_{smooth}$ = 3.22 (from Table 1)
Stub Length = 74.4 mil

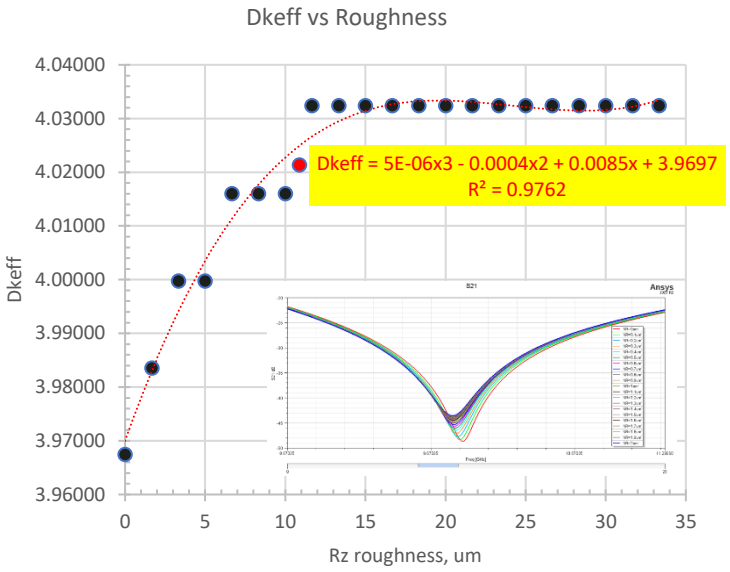
$$Dkeffxy_{rough} \cong \frac{\ln\left(\frac{40.04}{11.80}\right)}{\ln\left(\frac{40.04}{12.66}\right)} \times Dkeffxy_{smooth}$$

$$\cong 1.062 \times 3.22 \cong 3.42$$

Ref: [1] Scott McMorrow et al, "Anisotropic Design Considerations for 28 Gbps Via to Stripline Transitions", DesignCon 2015 proceedings, Santa Clara, CA.
[2] Scott McMorrow, "Anisotropy Test Vehicle Tachyon Results", Samtec presentation, 2022

Dkeff Increase from Inductance due to Via Roughness

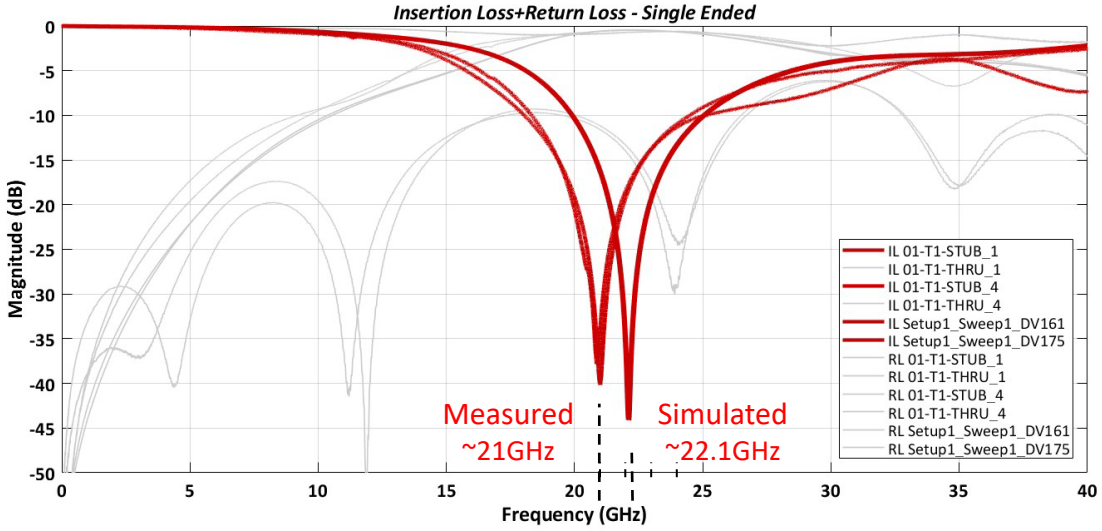
f_0 Hz	TD ps	NR um	Rz um	Dkeff	Dkeff % Delta
9.90E+09	25.25	0	0.00	3.9674	0.00%
9.88E+09	25.30	0.1	1.67	3.9835	0.41%
9.86E+09	25.35	0.2	3.33	3.9997	0.81%
9.86E+09	25.35	0.3	5.00	3.9997	0.81%
9.84E+09	25.41	0.4	6.67	4.0160	1.22%
9.84E+09	25.41	0.5	8.33	4.0160	1.22%
9.84E+09	25.41	0.6	10.00	4.0160	1.22%
			10.90	4.0213	1.36%
9.82E+09	25.46	0.7	11.67	4.0323	1.64%
9.82E+09	25.46	0.8	13.33	4.0323	1.64%
9.82E+09	25.46	0.9	15.00	4.0323	1.64%
9.82E+09	25.46	1	16.67	4.0323	1.64%
9.82E+09	25.46	1.1	18.33	4.0323	1.64%
9.82E+09	25.46	1.2	20.00	4.0323	1.64%
9.82E+09	25.46	1.3	21.67	4.0323	1.64%
9.82E+09	25.46	1.4	23.33	4.0323	1.64%
9.82E+09	25.46	1.5	25.00	4.0323	1.64%
9.82E+09	25.46	1.6	26.67	4.0323	1.64%
9.82E+09	25.46	1.7	28.33	4.0323	1.64%
9.82E+09	25.46	1.8	30.00	4.0323	1.64%
9.82E+09	25.46	1.9	31.67	4.0323	1.64%
9.82E+09	25.46	2	33.33	4.0323	1.64%



Drillϕ_{smooth} = 11.80 mil
Drillϕ_{rough} = 12.66 mil
Rz Roughness ~ 0.43 mil (10.9 um)
Antipadϕ = 40.04 mil
$Dkeff_{smooth}$ = 3.97
$Dkeff_{rough}$ = 4.02

$$\Delta = \left[\frac{4.0213}{3.9674} - 1\right] 100 = 1.36\% \text{ Increase}$$

Conclusion



$$Dkeff_{meas} = \left(\frac{1.18E10}{4\times 21.0E9\times 74.4E-3}\right)^2 \cong 3.6$$

$$Dkeff_{sim} = \left(\frac{1.18E10}{4\times 22.1E9\times 74.4E-3}\right)^2 \cong 3.2$$

$$\Lambda_{eff} = \frac{3.6}{3.2} - 1 = 12.5\%$$

Avg Anisotropy due to pressed thickness (Tabel 1)	4.9%
+ Dkeff due to C roughness	6.2%
+ Dkeff due to L roughness	1.36%
Total	12.5%

Based on cross-section data from extended case study - adjusting Dkeff for pressed thickness and via roughness adds ~ 8 % to the dielectric anisotropy

* Ref. [1] Scott McMorrow, "Anisotropy Test Vehicle Tachyon Results", Samtec presentation, 2022
[2] Scott McMorrow et al, "Anisotropic Design Considerations for 28 Gbps Via to Stripline Transitions", DesignCon 2015 proceedings, Santa Clara, CA.
[3] Bert Simonovich, "From Smooth to Imperfect Vias: The Rough Truth Impacting Simulation Model Accuracy", White Paper, June 1, 2025

What We Learned

- **Beyond material anisotropy, factors such as resin content, fabricated dielectric thicknesses, and drilled hole size contribute to variations in the effective dielectric constant surrounding via structures.**
- **Additionally, via barrel roughness affects both Dkeff and time delay, further complicating accurate dielectric modeling validation.**

References

- Bert Simonovich, “From Smooth to Imperfect Vias: The Rough Truth Impacting Simulation Model Accuracy”, White Paper, June 1, 2025
- Bert Simonovich, “A Heuristic Approach to Assess Anisotropic Properties of Glass-reinforced PCB Substrates”, DesignCon 2024 proceedings, Santa Clara, CA
- Scott McMorrow, “Anisotropy Test Vehicle Tachyon Results”, Samtec presentation, 2022
- Scott McMorrow et al, “Anisotropic Design Considerations for 28 Gbps Via to Stripline Transitions”, DesignCon 2015 proceedings, Santa Clara, CA
- Al Neves et al, “Free Signal Integrity? How Understanding Anisotropic Materials & Tolerances Could Increase Performance at 112/224Gbps & Beyond”, DesignCon 2025 proceedings, Santa Clara, CA
- Bert Simonovich, "A Practical Method to Model Effective Permittivity and Phase Delay Due to Conductor Surface Roughness", DesignCon 2017 proceedings, Santa Clara, CA

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